Process Change Notification Form

PCN Number:	PCN_0244
Date of Notification:	November 21, 2008
Cirrus Logic P/N(s):	CS4525-CNZ, CS4525-CNZR
Date PCN Effective:	February 20, 2009
Reason for Change:	☒ Design /New Rev. ☐ Fab Site ☐ Fab Process ☐ Additional Fab Source ☐ Assembly Site ☐ Assembly Process ☐ Additional Assembly Source ☐ Other (specify)
Description of Change:	☒ Fix errata ☐ Yield enhancement ☐ Fix known bug ☐ Performance Improvement ☐ Other ******See pages below******
Cirrus Logic P/N Change:	☐ Yes, New Part Number: ☒ No
Pack Mark Change:	☒ Yes ☐ No If Yes, briefly explain: **YFFAC0 to YFFAC1** *[Any Fab, Assembly, or Design changes results in pack mark changes, please provide detail]*
Lot Effective Date:	**Date Code 0817** *[Contact the area sales representative for availability of samples if applicable]*
Quality & Reliability impact:	******See pages below****** Qualification Data: ☒ Required ☐ Not Required
Datasheet Change Required?	☐ Yes ☒ No If Yes, briefly explain:
Software Change Required?	☐ Yes ☒ No If Yes, briefly explain:

Errata: CS4525 Rev. C0 Silicon

(Reference CS4525_DS726PP3 Data Sheet)

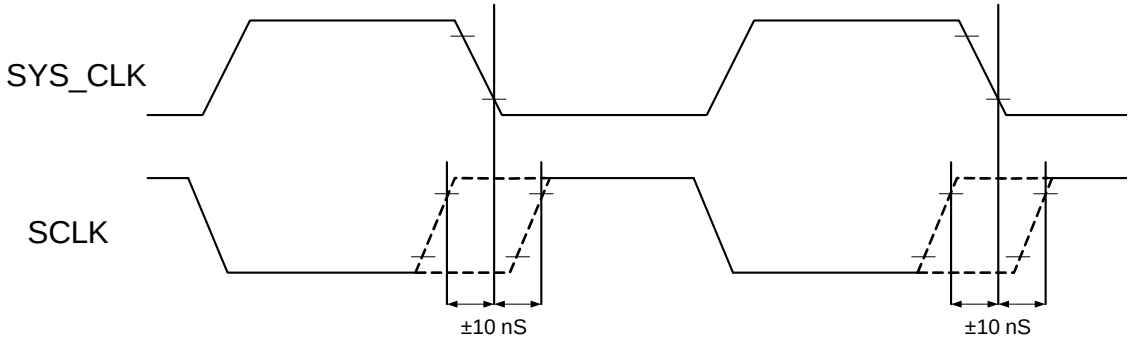
- In Software Mode, the total digital gain for each channel — including pre-scaler, tone control, parametric EQ, channel volume, and master volume — must not exceed +20 dB at any frequency.

- If the maximum voltage of VP can exceed 15.0 V, then the internal ramp feature must never be enabled and RmpSpd[1:0] must always be set to its default value of 11.

- The Thermal Foldback feature is disabled in Hardware Mode regardless of the state of the EN_TFB pin.

- If ADC input is selected, the Delay Port is enabled, and the Auxiliary Serial Output is configured for I2S format, then the Left and Right channels will be swapped on the AUX_SDOUT output, the logic-level PWM_SIGx outputs, and the high-power OUTx outputs. To correct for this, it is recommended to set RChMix[1:0] to 11 and LChMix[1:0] to 11 to swap the signals.

- When using the serial audio input port, timing variation in SCLK signal transitions relative to SYS_CLK signal transitions may result in a failure to detect the correct LRCK period by the sample rate converter. This can lead to increased THD+N, and is most evident when the SYS_CLK frequency is very nearly but not exactly an integer multiple of SCLK. When the device is operated with its serial audio input signals asynchronous to SYS_CLK, this phenomenon is mitigated if the serial audio input sampling rate is not evenly divisible into the SYS_CLK frequency. The phenomenon can be eliminated by supplying the device with serial audio input signals that are synchronously derived from SYS_CLK, with the rising edge of SCLK occurring within 10 ns of the corresponding falling edge of SYS_CLK as shown in Figure 1.



Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to http://www.cirrus.com

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Errata: CS4525 Rev. C1 Silicon

(Reference CS4525_DS726PP3 Data Sheet)

- In Software Mode, the total digital gain for each channel — including pre-scaler, tone control, parametric EQ, channel volume, and master volume — must not exceed +20 dB at any frequency.

- If the maximum voltage of VP can exceed 15.0 V, then the internal ramp feature must never be enabled and RmpSpd[1:0] must always be set to its default value of 11.

- The Thermal Foldback feature is disabled in Hardware Mode regardless of the state of the EN_TFB pin.

- If ADC input is selected, the Delay Port is enabled, and the Auxiliary Serial Output is configured for I2S format, then the Left and Right channels will be swapped on the AUX_SDOUT output, the logic-level PWM_SIGx outputs, and the high-power OUTx outputs. To correct for this, it is recommended to set RChMix[1:0] to 11 and LChMix[1:0] to 11 to swap the signals.

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RELIABILITY QUALIFICATION REPORT

Reliability Report: QRR081105

Subject/Purpose:

This is to qualify the CS4525-CNZ/C0/C1 device manufactured at MagnaChip (F) and ssembled in the Pb-free 48QFN package at Amkor K1 (Korea).

APPROVALS:

Rod Boutwell
Reliability Engineering

Results:

Qualification successful.

STATUS:

Complete - Pass

Stress	Conditions	Method	Duration	Lot	Results (Fail/Sample)
HTOL	125 °C	JESD22-A108	48 Hours	1	0/77
1251-1 (Similarity)	5.25 Volts		500 Hours	1	0/77
QJ1487	9 Volts		1000 Hours	1	0/77
QJ1609 (Similarity)	Dynamic				
			500 Hours	2	0/77
			1000 Hours	2	0/77
	125 °C		1072 Hours	2	0/77
	5.5 Volts				
	9 Volts		48 Hours	3	0/77
	Dynamic		500 Hours	3	0/77
			1000 Hours	3	0/77
ESD Human Body Model	25 °C	JESD22-A114	1500 Volts	1	0/5
QJ1399			2000 Volts	1	0/5
			2500 Volts	1	0/5
ESD CDM (Charged Device Model)	25 °C	JESD22-C101 700V corner pins, 500V all other pins	500/750 Volts	1	0/3
QJ1487			1000 Volts	1	0/3
Latch-Up VDD	85 °C	JESD78	7.95 Volts	1	0/3
QJ1399			27.30 Volts	1	0/3
Latch-Up I/O High Power Out1-4 pins	85 °C	JESD78	+1200 mA	1	0/3
QJ1399			-3000 mA	1	0/3

Background Information:

Part #: CS4525 **Rev:** C0/C1 **Fab:** MagnaChip (F) **Lead Finish:** Pb-free
Package: 48QFN **Assembly:** Amkor K1 (Korea)

Reliability Report: QRR081105

Stress	Conditions	Method	Duration	Lot	Results (Fail/sample)
Latch-Up I/O High Power RampCap pins QJ1399	85 °C	JESD78	+200 mA -200 mA	1 1	0/3 0/3
Latch-Up I/O Low Power pins QJ1399	85 °C	JESD78	+150 mA -150 mA	1 1	0/6 0/6
Precondition MSL-3 1197-1 (Similarity) 1229-1 (Similarity) QJ1465	24HR 125 °C Bake 192HR 30°C/60%RH Soak 3 pass 260 °C Convection reflow	JESD22-A113	Precondition Precondition Precondition	1 2 3	0/241 0/77 0/231
HAST 1197-1 (Similarity) QJ1465	130 °C 85 %RH 5.25 Volts 130 °C 85 %RH 5.25 Volts 9 Volts	JESD22-A110	96 Hours 96 Hours	1 2	0/77 0/77
Temperature Cycle cond. C 1197-1 (Similarity) QJ1465	-65 °C +150 °C air to air air to air	JESD22-A104	500 Cycles 500 Cycles	1 2	0/77 0/77
Tomography (CSAM) 1197-1 (Similarity) QJ1465		J-STD-035	500 TCC 500 TCC	1 2	0/5 0/5
Autoclave/PPOT 1229-1 (Similarity) QJ1465	121 °C 15 psig 100% R.H.	JESD22-A102	96 Hours 96 Hours	1 2	0/77 0/77

Background Information:

Part #: CS4525 **Rev:** C0/C1 **Fab:** MagnaChip (F) **Lead Finish:** Pb-free

Package: 48QFN **Assembly:** Amkor K1 (Korea)

Reliability Report: QRR081105

Stress	Conditions	Method	Duration	Lot	Results (Fail/sample)
Solderability 1229-1 (Similarity)	93 °C steam aging 8 Hours 245 °C solder bath 5 Seconds	JESD22-B102	Solderability	1	0/10
HTSL (High Temp Storage Life) 1197-1 (Similarity)	150 °C	JESD22-A103	500 Hours 1000 Hours	1 1	0/77 0/77

Background Information:

Part #: CS4525 **Rev:** C0/C1 **Fab:** MagnaChip (F) **Lead Finish:** Pb-free

Package: 48QFN **Assembly:** Amkor K1 (Korea)

CIRRUS LOGIC, INC., P.O. Box 17847, Austin, Texas 78760; 2901 Via Fortuna, Austin, Texas 78746, TEL: (512) 851-4000

Cirrus Logic PCN administrator: Cirrus Logic - Customer Quality

Digitally signed by Cirrus Logic - Customer Quality
DN: cn=Cirrus Logic - Customer Quality, c=US, ou=Cirrus Logic Austin, email=customer_quality@cirrus.com
Reason: All signatures on file
Date: 2008.11.24 14:00:06 -06'00'

Acknowledgement of Receipt of Notice:

Does customer waive PCN Effective Date? ☐ **YES** ☐ **NO**

Company Name: _____

Name (please print)**:** _____ **Title:** _____

Signature: _____ **Date:** _____

Customer Representative is to obtain the customer acknowledgement/signature and return this notification to Cirrus Logic Corp. Quality, attn: PCN administrator at fax number (512) 851-4656

NOTE: Lack of acknowledgement within 30 days of the date of notice, constitutes acceptance of change.
(Reference JEDEC Industry Standard: JESD-46)