Process Change Notification Form

PCN Number:	PCN_0262
Date of Notification:	06/01/2009
Cirrus Logic P/N(s):	CS4221-KS, CS4330-KS, CS4331-BS, CS4331-KS, CS4333-KS CS4341-KS, CS4392-KS, CS5012A-BL7, CS5014-BL14, CS5016-BL16 CS5101A-BL8, CS5101A-JL8, CS5102A-BL, CS5102A-JL, CS5126-KL CS5321-BL, CS5322-BL, CS5330A-BS, CS5501-BP, CS5501-BS CS5503-BP, CS5503-BS, CS5504-BP, CS5504-BS, CS5505-AP CS5505-AS, CS5506-BP, CS5506-BS, CS5507-AP, CS5507-AS CS5508-BP, CS5508-BS, CS5509-AP, CS5509-AS, CS5510-AS CS5511-BS, CS5512-BS, CS5513-BS, CS5516-AS, CS5520-BS CS5522-AP, CS5524-AP, CS5526-BP, CS5529-AP, CS61535A-IL1 CS61574A-IL1, CS61575-IL1
Date PCN Effective:	07/01/2009
Reason for Change:	☐ Design /New Rev. ☐ Fab Site ☐ Fab Process ☐ Additional Fab Source ☐ Assembly Site ☒ Assembly Process ☐ Additional Assembly Source ☐ Other (specify)
Description of Change:	☐ Fix errata ☐ Yield enhancement ☐ Fix known bug ☐ Performance Improvement ☒ Other: ANST will transfer all subcontracted Sn/Pb plating services from Technic Semiconductor Engineering, Suzhou to Welnew Microelectronics, Wuxi. • Applies to all leaded package families assembled at ANST (SOIC, PDIP, TSSOP, MSOP, PLCC) • Matte tin (Pb-free) plating is not affected by this change. • No other assembly processes are affected by this change.
Cirrus Logic P/N Change:	☐ Yes, New Part Number: ☒ No
Pack Mark Change:	☐ Yes ☒ No If Yes, briefly explain: *[Any Fab, Assembly, or Design changes results in pack mark changes, please provide detail]*
Lot Effective Date:	Lots manufactured with a date code of 0927 and later. *[Contact the area sales representative for availability of samples if applicable]*
Quality & Reliability impact:	Qualification Data: ☒ Required ☐ Not Required *****see pages below*****
Datasheet Change Required?	☐ Yes ☒ No If Yes, briefly explain:
Software Change Required?	☐ Yes ☒ No If Yes, briefly explain:

High-speed Sn-Pb plating evaluation report

WUXI WELNEW MICRO-ELECTRONIC CO., LTD.

PRESENTED BY
Cirrus Logic Reliability

June 8, 2009

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1 SAMPLE DESCRIPTION

Customer		ANST
Package/lead		PLCC32
Building Quantity	High-speed Sn-Pb Plating	**30strips**

2. PROCESS FLOW AND PARAMETER

High-speed Sn-Pb Plating process

Plating Machine	CEM	Wel-DP2-6MP-SNR
Electro-clean temp	50	°C
Electro-clean current	200	Ampere
Electro-clean Time	108	Sec
Descale time	33	Sec
Water jet pressure	100	Kg/cm2
Pre-dip	9	Sec
Plating current	50	Ampere
Plating temp.	40	°C
Plating time	96	Sec
Belt speed	2.5	m/Min
Plating chemistry	ROHMHAAS	SC
Neutralization temp.	ROOM	°C
Hot DI water temp.	60	°C

3. Chemical analysis

Process	Chemical	Spec	Analysis result
ED	**KOH**	**150-250 [g/l]**	**196[g/l]**
Descale	**S-7025**	**150-250[ml/l]**	**205[ml/l]**
Pre-dip	**MSA**	**90-130[ml/l]**	**110[ml/l]**
Plating	**TIN**	**30-60 [g/l]**	**55 [g/l]**
	LEAD	**6~10 [g/l]**	**8g/l**
	MSA	**220-280ml/l**	**256ml/l**
	SC PRIMARY	**80-120[ml/l]**	**85 [ml/l]**
	SC SECONDARY	**3-6 [ml/l]**	**5[ml/l]**
	RD	**15-30 [ml/l]**	**20 [ml/l]**
Neutralize	**NO TARN SN-2**	**20-40[ml/l]**	**31[ml/l]**

PLCC32 lead tin plating thickness and composition

			unit: uinch					unit: Sn%wt	
Thickness									
13.8	14.1	13.7	14.1	11.4	87.2	87.8	87.7	88.0	88.6
13.1	14.2	13.9	14.2	13.2	87.5	87.6	89.6	87.8	88.0
12.2	12.3	12.8	14.0	14.2	88.3	87.4	87.5	87.4	87.6
11.7	12.2	12.3	12.1	13.1	87.8	87.9	87.5	88.2	88.3
14.2	14.5	14.5	11.8	12.5	87.7	87.2	88.2	88.8	88.5
15.8	13.5	13.3	14.3	14.6	87.8	86.7	87.2	87.0	87.7
Spec		7.62~17.8			80~95%				
Min		11.4							
Max		15.8							
Average		13.39							
Cpk		1.69							

4.2 Solderability test

Plating	High-speed Pure Tin
Pkg/Id	**PLCC32**
Sample size	**10 units**
Solder alloy	**SnPb**
Precondition	**Steamaging 8hours Baking 2hours**
Solder pot temp	**245^{0}C**
Flux used	**R-type non-activate**
Flux immersion	**5 sec**
Dwell time	**5 sec**
Result	**0/10**

4.3 Lead adhesion

Pkg/Id	S/S	Baking condition	Microscope	Test result
				Peeling
PLCC32	10leads	175˚C/1Hr	30X	0

4.4 Tape peeling test

Pkg/Id	S/S	Microscope	Test result
			Peeling
PLCC32	3units/PKG	30X	0

Cirrus Logic PCN administrator: Cirrus Logic - Customer Quality

Digitally signed by Cirrus Logic - Customer Quality
DN: cn=Cirrus Logic - Customer Quality, c=US, ou=Cirrus Logic Austin, email=customer_quality@cirrus.com
Reason: All signatures on file
Date: 2009.0[illegible]:55 -05'00'

Date: _____

Acknowledgement of Receipt of Notice:

Does customer waive PCN Effective Date? ☐ **YES** ☐ **NO**

Company Name: _____

Name (please print)**:** _____ **Title:** _____

Signature: _____ **Date:** _____

Customer Representative is to obtain the customer acknowledgement/signature and return this notification to Cirrus Logic Corp. Quality, attn: PCN administrator at fax number (512) 851-4656

NOTE: Lack of acknowledgement within 30 days of the date of notice, constitutes acceptance of change. (Reference JEDEC Industry Standard: JESD-46)