Jauch
THE PULSE OF PROGRESS

CRYSTAL CIRCUITS AND OPTIMIZATION

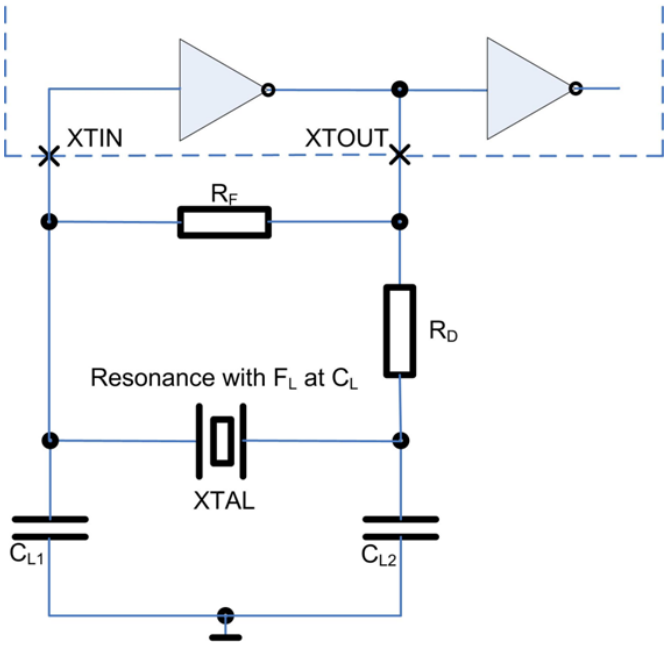
DOCUMENT

CONTENT

1. Crystal oscillator – basic circuits

- Pierce circuit with load capacitance C_L
- Phase shift by inverter amplifier = 180°
- Phase shift by crystal with C_L at load resonance frequency F_L = 180°
- Positive feedback is 1st condition for oscillation
- Amp: gain ≥ losses of resonant circuit is 2nd condition for oscillation
- R_D to control the crystal power
- R_F defines DC operating condition for amplifier

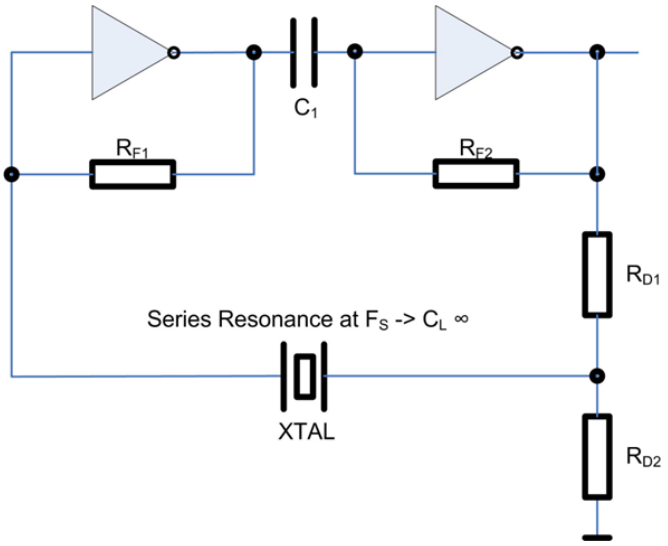
- Specification for nominal load capacitance C_L for usage in this type of circuit is essential!



Pierce circuit

- Series resonant circuit (no load capacitance, load capacitance ∞)
- Phase shift by inverter amplifier = 360°
- Phase shift by crystal at series resonant frequency F_S = 0°
- Positive feedback is 1st condition for oscillation
- Amp. gain ≥ losses of resonant circuit is 2nd condition for oscillation
- R_{D1} , R_{D2} to control crystal power
- R_{F1} , R_{F2} define DC operating condition

- Information of usage in this type of series resonance circuit is essential!

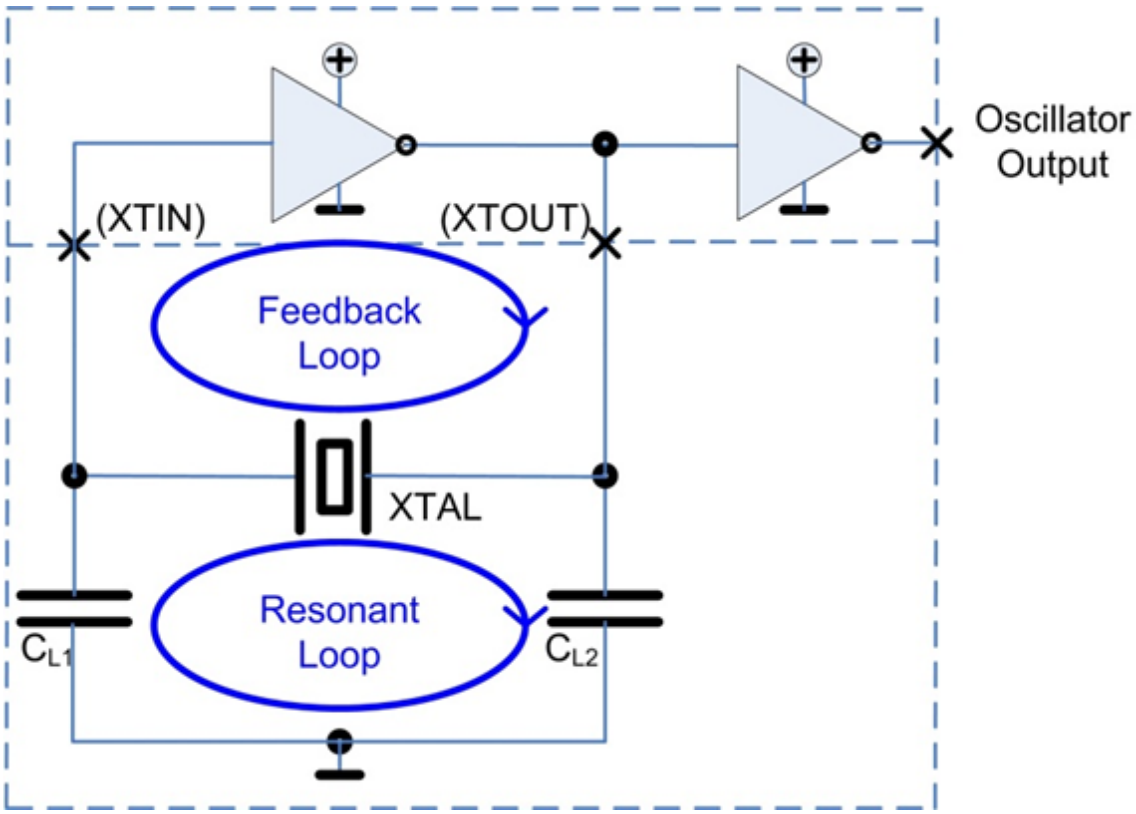


Crystal circuit for series resonance (simplified)

2. Crystal oscillator circuit

- Resonant loop:
  - o Crystal (XTAL) and load capacitors (C_{L1} a. C_{L2})
  - o Load resonant frequency determined by crystal, load capacitor(s)
  - o Equivalent Series Resistor (ESR) of crystal → energy loss

- Feedback loop:
  - o Inverting amplifier, amplifies signals at XTIN to XTOUT by a certain gain
  - o Amp. gain is required to compensate losses in resonant loop
  - o If loss is 0.5, amp. gain must be 2 minimum (better more for margin)
  - o Additional condition: total phase shift of feedback signal



3. Considerations for load capacitance CL

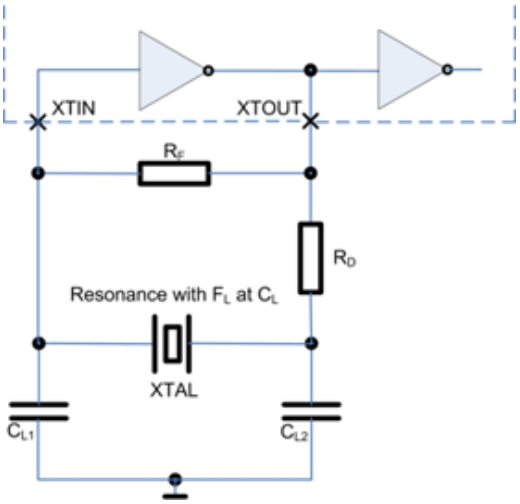
- For Pierce circuit – crystal is given with nominal load capacitance C_{LNom}
- Theoretical approach does not take stray capacitance, pin capacitance etc. into account

$$C_{LTh} = \left[\frac{C_{L1} * C_{L2}}{C_{L1} + C_{L2}} \right]$$

theoretical value C_{LTh} excluding stray and pin capacitance

- Due to the stray and pin capacitance, the load capacitance CLth built by C_{L1}, C_{L2} must be smaller than the nominal load capacitance C_{LNom} of the crystal
- Empirical value for overall stray capacitance CLSt is 4pF ~ 6pF
- Calculation of required load capacitors C_{L1}, C_{L2} taking overall stray capacitance C_{LSt} and given nominal load capacitance C_{LNom} into account

$$C_{LTh} = \left[\frac{C_{L1} * C_{L2}}{C_{L1} + C_{L2}} \right] = C_{LNom} - C_{LSt}$$



- The total effective load capacitance should be equal to the nominal load capacitance C_{LNom} of the crystal!

- For Pierce circuit – estimation of the load capacitance C_{LNom} to be specified to the crystal supplier:

$$C_{LTh} = \left[\frac{C_{L1} * C_{L2}}{C_{L1} + C_{L2}} \right]$$

theoretical value for C_{LTh} excluding stray and pin capacitance

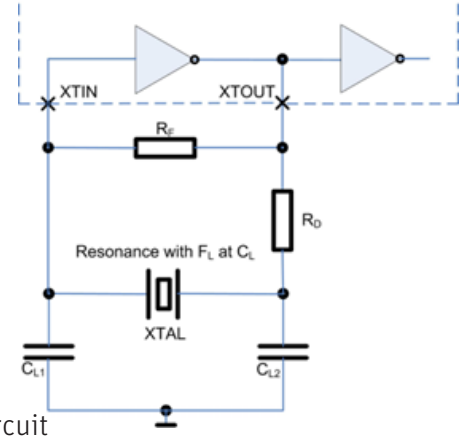
- Total effective load capacitance $C_{Leff} > C_{Lth}$ due to stray and pin capacitance
- Empirical value for overall stray capacitance C_{LSt} is 4pF ~ 6pF

$$C_{Leff} = C_{LSt} + \left[\frac{C_{L1} * C_{L2}}{C_{L1} + C_{L2}} \right]$$

total effective load capacitance C_{Leff} for crystal

- Total effective load capacitance C_{Leff} should be equal to the nominal load capacitance C_{LNom} of the crystal!

Example: crystal with C_{LNom} = 12pF → C_{Leff} = 12pF
assumption C_{LSt} = 4pF → 8pF required by C_{L1} and C_{L2}
→ C_{L1}, C_{L2} each 16pF



Pierce circuit

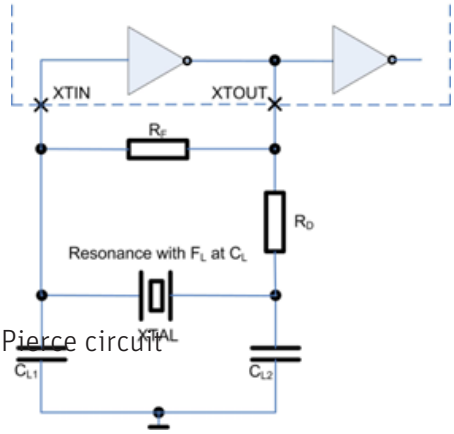
4. Mismatching of load capacitance CL

- Estimation of the frequency error if C_L is mismatched:

$$\Delta f_L = \left[\frac{C_1}{2} * \left(\frac{1}{(C_0 + C_{Leff})} - \frac{1}{(C_0 + C_{LNom})}\right)\right] * 10^6 \; in \; [ppm]$$

- C_{Leff} is the total effective value including stray and pin capacitance, C_{LNom} is the specified / nominal value of the load capacitance CL

- C_0, C_1 specific crystal equivalent data
- C_0, C_1 are values depending on crystal package and frequency
- C_0, C_1 can be determined by a dedicated crystal analyzer



Pierce circuit

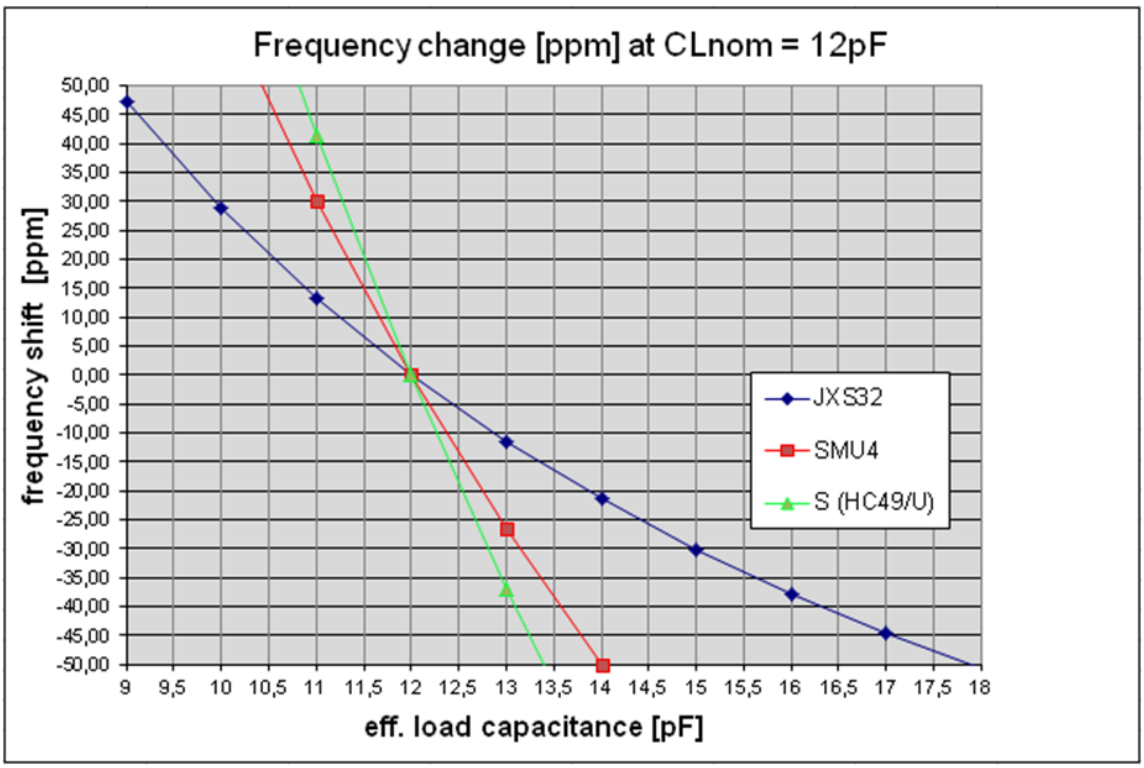
- Frequency shift caused by mismatching of load capacitance CL!
- Estimation possible by formula

$$\Delta f_L = \left[\frac{C_1}{2} * \left(\frac{1}{(C_0 + C_{Leff})} - \frac{1}{(C_0 + C_{LNom})}\right)\right] * 10^6 \; in \; [ppm]$$

- C_0, C_1 specific by crystal frequency and package
- C_{LNom} specified value, C_{Leff} total effective load capacitance

Package	miniature crystal	SMD crystal	pin type crystal
Jauch...	JXS32	SMU3	S (HC49/U)
frequency	26.0MHz	25.0MHz	26.0MHz
nominal C_L	12pF	12pF	12pF
C_0	1.4pF	3.2pF	5.9pF
C_1	4.4fF	13.9fF	25.0fF
C_L tolerance (12pF -10%)	10.8pF	10.8pF	10.8pF
frequency shift	+16.2ppm	+36.8ppm	+50.2ppm
C_L plus 3pF stray cap.	15pF	15pF	15pF
frequency shift	-30.0ppm	-70.8ppm	-100.2ppm

- Frequency shift due to mismatching of load capacitance C_L!
- C_0, C_1 specific according to crystal package and frequency
- C_{L2} specified value, C_{L1} total effective load capacitance



5. Series resistance (ESR) for small crystals

Series resistance (ESR) increases for small crystal packages

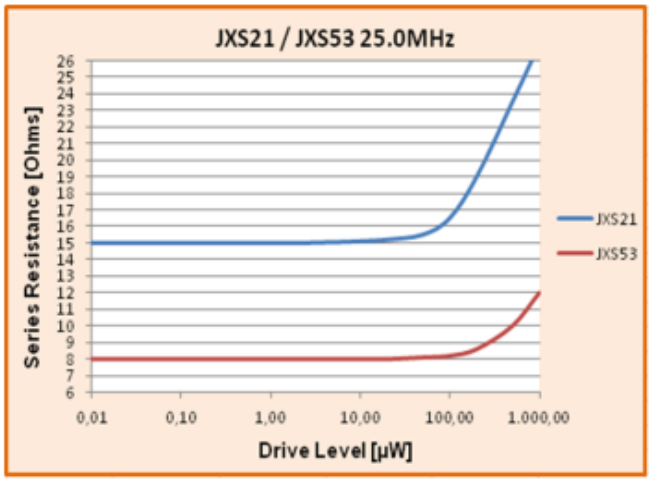
Package	Dimension [mm]	Frequency [MHz]	Series Resistance [%, relative]
JXS75	7.0 x 5.0	25.0	100
JXS53	5.0 x 3.2	25.0	100
JXS32	3.2 x 2.5	25.0	160
JXS22	2.5 x 2.0	25.0	200
JXS21	2.0 x 1.6	25.0	300

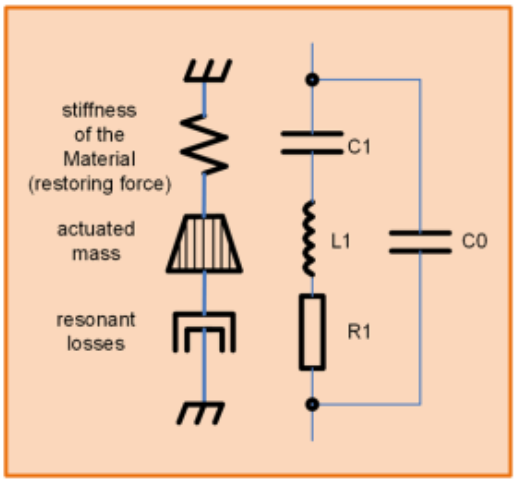
Lowest available frequency increases for small crystal packages

Package	Dimension [mm]	Minimum frequency [MHz]
JXS75	7.0 x 5.0	5.0
JXS53	5.0 x 3.2	8.0
JXS32	3.2 x 2.5	10.0
JXS22	2.5 x 2.0	16.0
JXS21	2.0 x 1.6	20.0

6. Drive Level Dependency (DLD)

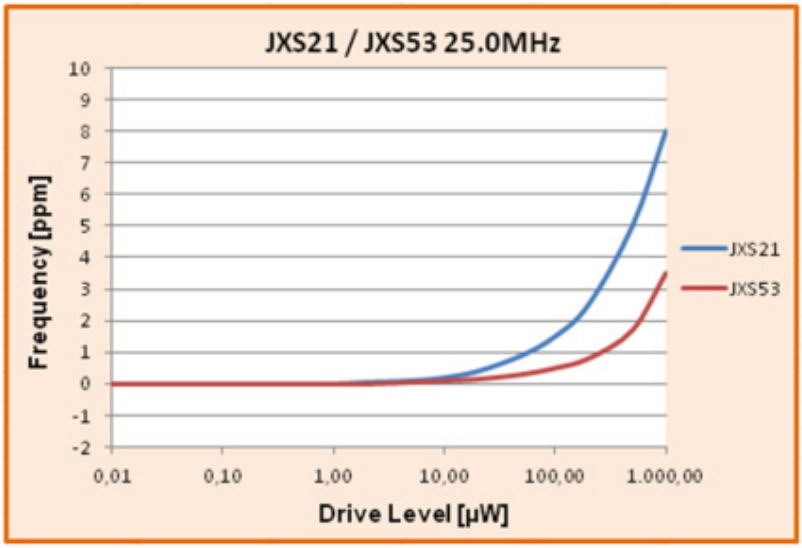
- A crystal is a mechanical resonator with losses
- R1 is electrical equivalent value representing mechanical losses
- At overload → the operation is no longer in the range of harmonic resonance
- Nonlinear losses cause increase of ESR at power levels exceeding power limits
- At extreme overload → crystal heats up → damage to crystal plate





7. Frequency Level Dependency (FLD))

- At overload → the crystal operation is no longer in the range of harmonic resonance
- Frequency shifts occur at power levels exceeding specified limits (depending on crystal package and frequency)

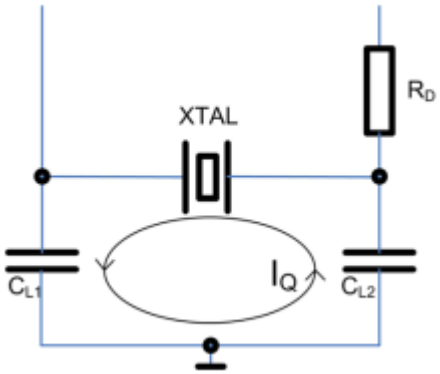


8. Load capacitance and resonant current

- Resonant loop is built by crystal (XTAL) and load capacitance C_{L1}, C_{L2}
- 2 load capacitors C_{L1}, C_{L2} build the load capacitance C_{LTh}

$$C_{LTh} = \left[\frac{C_{L1} * C_{L2}}{C_{L1} + C_{L2}} \right]$$

- Current in resonant loop IQ depends on impedance XC of load capacitance C_L
- Current and crystal power increase with larger C_L
- Small crystals have a lower maximum power specification and a higher ESR
- This can cause a problem for small crystal packages and too high C_L!



9. Measurement of crystal power PQ

- Theoretical calculation of I_Q and P_Q difficult
- Technical specifications / properties of output XTOUT are often not disclosed
- Position of stray capacitances may be unknown

- To determine I_Q and P_Q, the measurement of I_Q by a miniature current probe is most accurate

$$P_Q = R_L * (I_{Qrms})^2 = R_L * \left(\frac{I_{Qpp}}{2 * \sqrt{2}} \right)^2 = R_L * \frac{(I_{Qpp})^2}{8}$$

- R_L = transformed load resonance resistance at load capacitance C_L
- R_1 = equivalent series resonance resistance at $C_L = \infty$

$$R_L = R_1 * \left(1 + \frac{C_0}{C_L} \right)^2$$

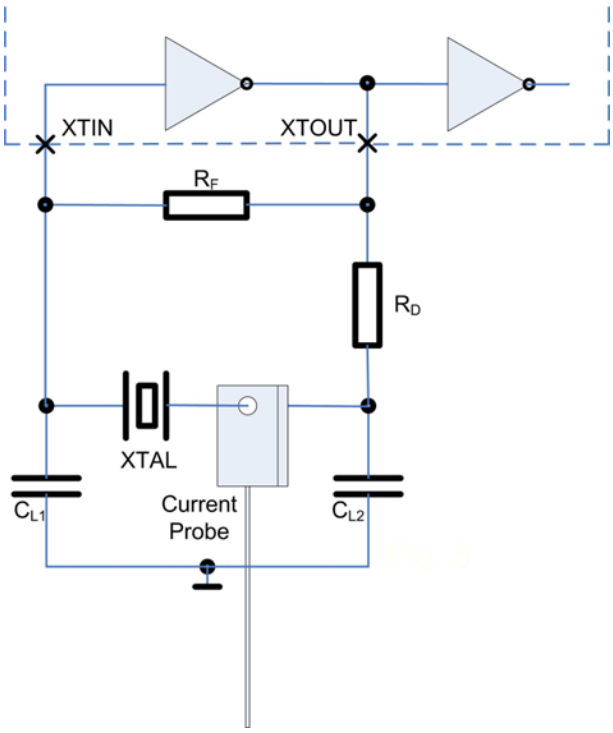


Fig. 5

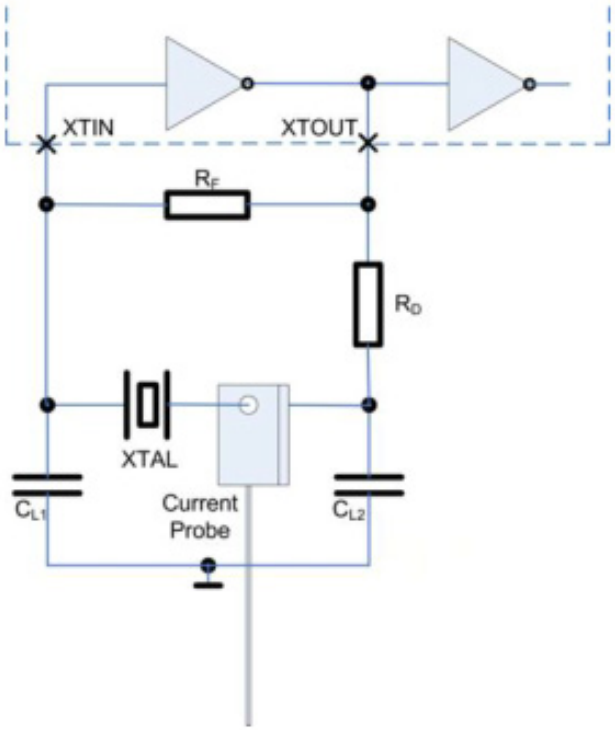
10. Reduction of crystal power PQ

- Small crystal packages → higher resonant losses,
  → higher equivalent series resistance R_1

- Large voltage swing, large C_L, no damping resistor R_D
- Too high a crystal power for small crystals is possible or even likely

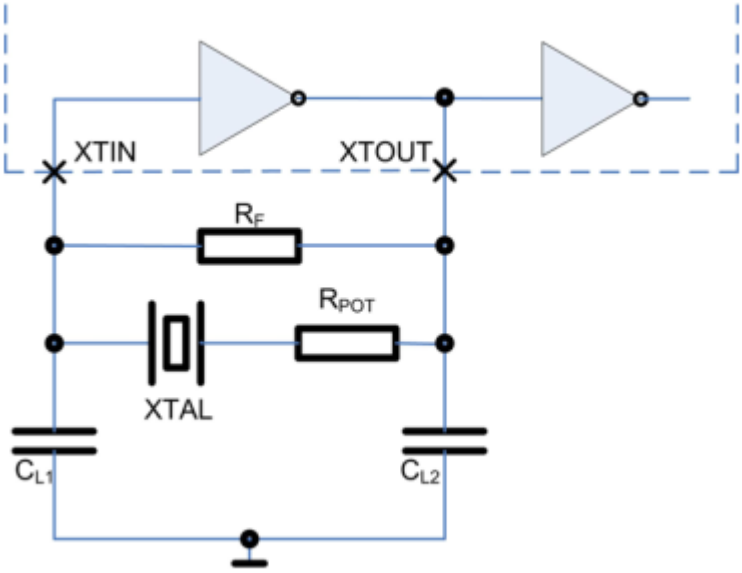
- To prevent crystal overloading
- Select a smaller C_L (for example 12pF for JXS32)
- Don't forget a position for R_D in your design

Note
- Damping resistor R_D reduces the loop gain!



11. Oscillation Safety Factor (OSF)

- Target: ensure reliable oscillation startup and operation
- Criteria for reliable oscillation: overall loop gain > 1 and correct overall phase shift; i.e. positive feedback in loop
- OSF condition with margin: OSF > 5 for consumer
  OSF > 10 for industrial & automotive



- Experimental determination of OSF with added resistor R_{POT}
- An increased ESR of the crystal is simulated by R_{POT}
- Increase R_{POT} setting, until oscillation ceases, measure R_{POTmax}.
- Calculate transformed load series resistance R_L of specific crystal sample at specific load conditions C_{Leff} found in the circuit
- Calculate transformed max. load series resistance RLmax according to crystal data sheet

$$R_L = R_1 * \left(1 + \frac{C_0}{C_{Leff}}\right)^2 \qquad R_{Lmax} = R_{1max} * \left(1 + \frac{C_0}{C_{Leff}}\right)^2$$

- Note: Total effective load capacitance CLeff in circuit and crystal parameters R1 and C0 must be known / measured by the crystal analyser!

- Calculate OSF

$$OSF = \frac{(R_L + R_{Potmax})}{R_{Lmax}}$$

- OSF margin: OSF > 5 or 10!

12. Searching for the best compromise

Requirements:

- Keep the crystal power within specified limits, also for small crystal packages
- Match total effective load capacitance to avoid frequency shifts
- Keep OSF margin: OSF > 5 or 10!

Conditions:

• Small crystal packages	→ relatively high equivalent series resistance $R_{1max.}$
• Higher series resistance	→ crystal power potentially too high, might require modification of crystal circuit
• Higher series resistance	→ reduction of loop gain and OSF
• Too high C_L	→ might cause too high crystal power
• Too small C_L	→ large tuning sensitivity, risk of frequency shift due to C_L Mismatching
• Damping resistor RD	→ reduction of crystal power, but also… → undesired reduction of OSF

Proposal:

- Close cooperation with Jauch Quartz at your early circuit design stage.

13. Mismatching of load capacitance CL - TF

- Frequency shift for tuning fork crystals caused by mismatching of load capacitance C_L !
- Estimation possible by formula

$$\Delta f_L = \left[\frac{C_1}{2} * \left(\frac{1}{(C_0 + C_{Leff})} - \frac{1}{(C_0 + C_{LNom})} \right) \right] * 10^6 \; in \; [ppm]$$

- C_0, C_1 specific by tuning fork package
- C_{LNom} specified value, C_{Leff} total effective load capacitance

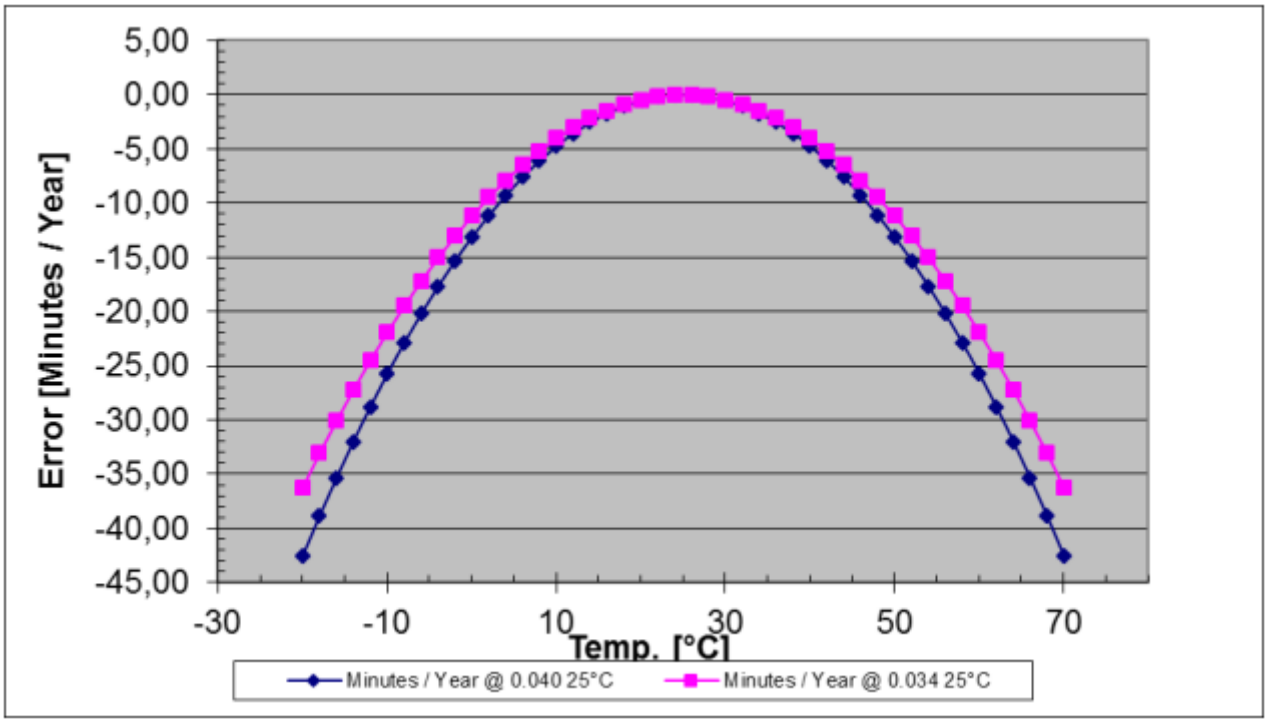
Package	SMD Tuning Fork	SMD Tuning Fork	SMD Tuning Fork
Jauch...	SMQ32SL	SMQ32SL	SMQ32SL
frequency	32.768kHz	32.768kHz	32.768kHz
nominal C_L	12.5pF	9pF	6pF
C_0	1.3pF	1.3pF	1.3pF
C_1	2.95fF	2.95fF	2.95fF
C_L tolerance (nom. -10%)	11.25pF	8.1pF	5.4pF
frequency shift	+10.7ppm	+13.7ppm	+18.1ppm
C_L plus 2pF stray cap.	14.5pF	11.0pF	8pF
frequency shift	-13.6ppm	-23.3ppm	-43.5ppm

Package	SMD Tuning Fork	SMD Tuning Fork	SMD Tuning Fork
Jauch...	JTX310	JTX310	JTX310
frequency	32.768kHz	32.768kHz	32.768kHz
nominal C_L	12.5pF	9pF	6pF
C_0	0.92pF	0.92pF	0.92pF
C_1	3.5fF	3.5fF	3.5fF
C_L tolerance (nom. -10%)	11.25pF	8.1pF	5.4pF
frequency shift	+13.4ppm	+17.6ppm	+24.0ppm
C_L plus 2pF stray cap.	14.5pF	11.0pF	8pF
frequency shift	-16.9ppm	-29.5ppm	-56.7ppm

14. Temperature Coefficient of Tuning Fork

- Temperature Coefficient defined by resonant mode: flexural resonator
- F/T can be calculated by formula, temp. coefficient is -0,04 max.; -0,034 typ.

$$\frac{\Delta f}{f} = TK * (+25°C - T)^2 \; in\,[ppm]$$



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